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Review article

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Thermal management materials for 3D-stacked integrated circuits

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Abstract

As transistor scaling approaches nanometre and even atomic scales, 3D stacking has become a critical enabler for advancement in the semiconductor industry, especially in high-performance computing and artificial intelligence (AI) applications. However, 3D integration introduces substantial thermal management challenges related to the increased power density and constrained heat dissipation pathways, particularly through low thermal conductivity interlayer dielectrics and complex interfaces. In this Review, we discuss state-of-the-art thermal management materials, covering their process compatibility, the critical integration challenges and the need for improved methods to enhance heat transport across interfaces. Advanced thermal characterization metrologies are introduced to highlight the need for non-destructive in-line metrologies. Finally, we provide a road map that outlines future research directions for material growth, integration and characterization methodologies to enable viable thermal solutions for 3D integration and beyond.

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Key points

- The shrinking dimensions, increased structural complexity and 3D stacking of silicon-based semiconductor devices are intensifying challenges in thermal dissipation.
- Breakthroughs are needed to address maximum temperatures near hot spots in 3D-stacked devices, requiring innovation in material growth, processing and integration.
- Advancements are necessary in the characterization of the thermal properties of the materials and in the methods to enhance heat transport across interfaces.
- The development of non-destructive in-line metrologies compatible with semiconductor processing flows is highly desirable for the characterization of thermal management film stacks and the monitoring of thermal dissipation performance within chips.

Introduction

Microelectronic chips based on integrated circuits (ICs) have been instrumental in driving technological breakthroughs across a wide range of modern applications including artificial intelligence (AI), high-performance computing, 5G/6G wireless communication, autonomous driving, the Internet of Things and more[1]. At the heart of these chips lies the field-effect transistor (FET), which has served as the fundamental building block and has undergone remarkable transformations since its invention in the 1920s. Complementary metal–oxide–semiconductor (CMOS) devices have become the dominant technology in the semiconductor industry. Continuous enhancements in power, performance and area efficiency have been the core driver of progress in CMOS-based ICs[2].

The IC industry has witnessed profound progress in transistor dimension shrinkage through advancement in lithography technologies since the early 1970s. After the 2010s, CMOS device architecture has evolved from planar to the fin field-effect transistor (FinFET) and further to the nanosheet field-effect transistor (NSFET), also known as gate-all-around, aiming to enhance electrostatic control[3]. The progression of device architecture is anticipated to continue with complementary field-effect transistors (CFETs), which stack n-type and p-type FETs vertically to offer potentially up to a twofold increase in transistor density[4] (Fig. 1a). Compared with the FinFET, where the silicon channel is directly connected to the bulk silicon substrate serving as an effective heat sink, the architectures of the NSFET and CFET introduce more heterogeneous interfaces that impede heat transport across materials[5].

Additionally, advanced NSFET and CFET designs have adopted the backside power delivery network (BSPDN) as a solution to alleviate routing congestion. This approach involves substantially thinning the bonded silicon down to submicrometre or even nanometre ranges prior to subsequent backside processing. The bonding layer, often made of silicon oxide with low thermal conductivity, adds an additional thermal barrier between the heat sink and the device substrate. Compared with a front-side power delivery network (FSPDN)-only architecture, BSPDN implementation could result in approximately 30% higher device self-heating temperatures[6] (Fig. 1b). In short, dissipating the heat generated by devices with complex architectures remains challenging, and thermal management in BSPDN-implemented NSFETs and CFETs has essential roles for device performance.

At the system level, 3D stacking of chips with diverse functions has emerged as the key enabler for high-performance computing and AI[7] (Fig. 1c). The 3D stacking of high-performance ICs offers a promising solution to meet the increasing demands of computing workloads. However, as more layers of active devices are stacked, managing heat dissipation becomes increasingly challenging[8].

As semiconductor devices continue to scale and embrace complex architectures such as 3D integration and nanoscale features, efficient thermal management has become a critical challenge. Self-heating in devices results in localized hot spots, particularly near the drain edge in front-end-of-line (FEOL) device regions. Scaled metal interconnects face increased joule heating within the back-end-of-line (BEOL) stack[9], which contributes to higher electrical resistance. Additionally, the thermal insulation provided by conventional interlayer dielectric materials further hampers heat dissipation, worsening localized hot spot issues[10] (Fig. 1d). These challenges lead to elevated junction temperatures, degraded device performance and a higher likelihood of premature failure[11].

In CMOS devices, many key electrical and reliability metrics are highly sensitive to temperature. Characteristics such as leakage currents and subthreshold slope are strongly influenced by elevated temperatures[12]. Reliability issues, including p-MOS negative bias temperature instability, gate dielectric degradation and time-dependent dielectric breakdown, are closely tied to thermal stresses during operation[13,14]. As devices continue to miniaturize, the integration of additional tiers into 3D architectures amplifies these thermal constraints, necessitating new approaches to heat management.

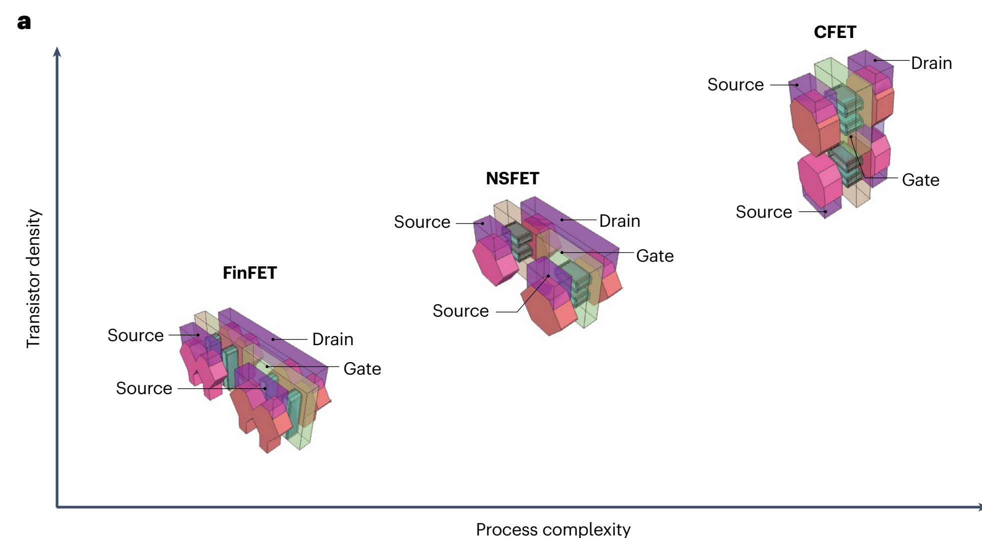
Despite the importance of these thermal effects, research remains limited in connecting innovative materials and processing techniques to the electrical behaviour of devices. Bridging this gap requires a deeper understanding of thermal transport mechanisms and their coupling to electrical performance. This insight is essential for developing optimized materials and integration strategies that can address the stringent thermal demands of next-generation semiconductor devices, ensuring robust performance and reliability.

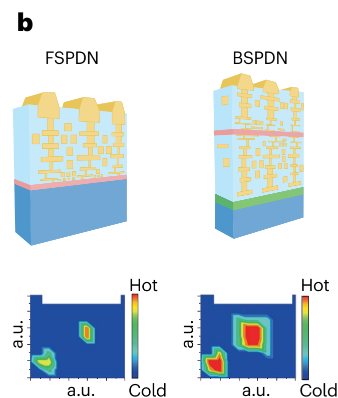
In this Review, we survey state-of-the-art thermal management materials, categorizing them by electronic properties and functional roles. We explore their process compatibility and integration challenges, with a focus on interfacial thermal boundary resistance (TBR), which is increasingly becoming a performance bottleneck. Additionally, we review advanced metrologies — both electrical and optical — used to characterize thermal conductivity and TBR across relevant length scales. Finally, we discuss critical integration challenges and propose future directions to enable efficient thermal dissipation in the AI era.

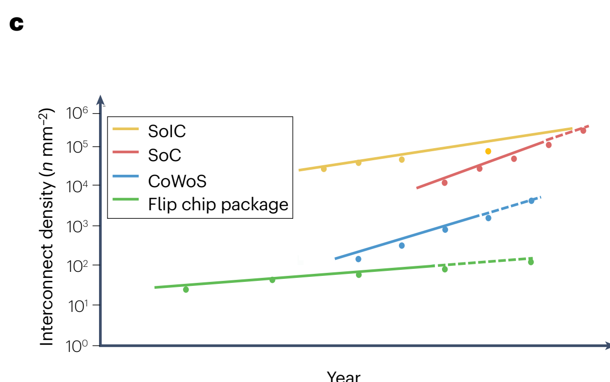
Fundamentals of heat transport in silicon-based devices

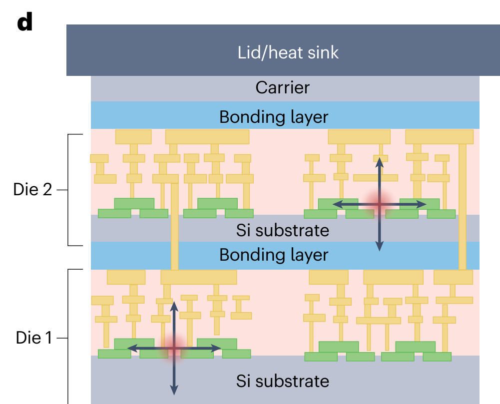
To cool the generated hot spots, heat must be transferred from the point of generation or local maximum along a thermal gradient in the system. The two most important material properties for heat transfer are heat capacity — the ability of a material to absorb heat (described in joules per kelvin) — and thermal conductivity — the ability of a material to transport heat (described in watts per metre per kelvin). In electronic materials, electrons and phonons are the primary contributors to these two material properties. Electrons are widely known as the free-charged

particles present in semiconductors and metals. Phonons are a quantized description of bond vibrations in a material that have dispersion relations similar to those of electrons. Heat capacity represents the change in internal energy of a system over time, which is why it is primarily relevant to transient heat transfer. In each material, the total internal energy can be described as the sum of the electronic and phonon contributions. The thermal conductivity of a material can be written as follows:









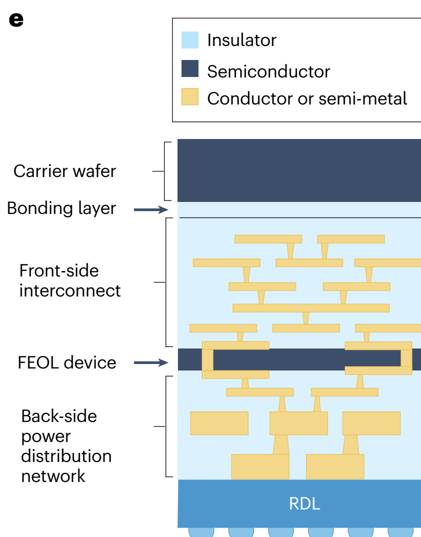


Fig. 1 | Device architecture and system integration induced thermal dissipation issues. a, Evolution of modern device architectures – from the fin field-effect transistor (FinFET) to the nanosheet field-effect transistor (NSFET) to the complementary field-effect transistor (CFET). Part **a** adapted with permission from ref. 1, IEEE. **b**, Comparison of the front-side power delivery network (FSPDN) and backside power delivery network (BSPDN) with corresponding temperature distribution. In the BSPDN design, heat-generating transistors (pink layer) are further thermally isolated from the silicon heat sink. The temperature map shows local hot spots with higher temperature in a BSPDN-implemented chip. Part **b** is reprinted with permission from ref. 6, IEEE **c**, System-level packaging evolution for high-performance computing. Part **c** adapted with permission from ref. 1, IEEE **d**, Typical hot spot locations in a 3D integrated circuit (IC). **e**, Potential insertion layers for thermal management materials in a device implementing a BSPDN. CoWoS, chip-on-wafer-on-substrate; FEOL, front-end-of-line; RDL, redistribution layer; SoC, system-on-a-chip; SoIC, small outline integrated circuit.

$$\kappa = \frac{1}{3}\left[C_{v,e}\upsilon_f\lambda_e + C_{v,p}\upsilon_p\lambda_p\right] \quad (1)$$

where $C_{v,e}$ and $C_{v,p}$ are the heat capacity of the electron and phonon, respectively; υ_f is the Fermi velocity of electrons in the system; υ_p is phonon velocity; and λ_e and λ_p are the mean free path of the electron and phonon, respectively.

In metallic materials, thermal transport is primarily mediated through electrons. In insulating materials where interatomic bonding is strong but very few free electrons are present, phonons facilitate thermal transport primarily. At boundaries between materials, thermal transport is facilitated primarily by electron-to-electron transfer or phonon mode matching. Although all boundaries add thermal resistance to a system, those between metals and insulators and those between materials with little overlap in phonon dispersion tend to have greater TBR.

In modern semiconductor devices and architectures, materials with different physical, chemical and thermal properties are used to optimize device performance, all of which exacerbate thermal issues by introducing thermal boundaries into the path of heat transfer. In addition, because of the size dependence of film thermal conductivity, many of the materials such as silicon and germanium in these architectures also exhibit notable lower effective thermal conductivities than those predicted in bulk forms. Phonon contributions to thermal conductivity are a function of mean free paths (Eq. 1). The transition from diffusive to ballistic phonon transport occurs when the characteristic length scale of nanostructures becomes comparable with or smaller than the phonon mean free path[15,16]. As a result, in some common semiconductor materials such as silicon, thin film thermal conductivity can be 50% lower than in bulk if the characteristic length scale shrinks down to <100 nm[17]. Finally, innovations such as strained channels, although vital for increasing mobility, also contribute to emergent thermal issues. As the phonon dispersion of a given material is a result of its bonding and resulting crystalline structure, any change to the structure results in changes to the thermal conductivity. In the case of silicon thin films, tensile strain decreases thermal conductivity whereas compressive strain increases thermal conductivity by 15–25%[18]. On the other hand, defects and disorders in materials induce phonon scattering and could further impact thermal conductivity[19].

Heat-spreading materials have long been used at the packaging level and in high-power and high-frequency electronics to manage hot spots. To overcome the highly confined architectures of future IC designs, high thermal conductivity heat-spreading materials are needed to dissipate hot spots and protect devices. These materials must have high thermal conductivity, can be deposited or integrated in a way that is compatible with current semiconductor manufacturing methods and have a consistent and accurate measurement method to enable development and testing.

Table 1 | Thermal properties of the thermal management materials

Material	Bandgap (eV)	Measured thermal conductivity ($W\,m^{-1}K^{-1}$)	Best interface achieved (TBR ($m^2\,K\,GW^{-1}$); TBC ($MW\,m^{-2}\,K^{-1}$))
Single-crystal diamond	5.47	1,700–2,400 (refs. 25,26)	20 m^2KGW^{-1} GaN/diamond[55]
Polycrystalline diamond (PCD)	–	2,200 cross-plane[58–60] 1,600 isotropic[61]	<1 m^2KGW^{-1} Si/diamond[68,69]
Diamond-like carbon (DLC)	–	1–5 (refs. 73–75)	–
Aluminium nitride (AlN)	6.1	<300 (refs. 76,78,81–94)	300 $MWm^{-2}K^{-1}$ AlN/SiO_2 (ref. 81)
Boron nitride (BN)	6	200–750 in plane, <5 cross-plane[104,105,107–109,112–118]	–
Silicon carbide (SiC) (4H/(6H)	3.26 (4H) 3.02 (6H)	345–415 in plane 320–390 cross-plane[124,125]	>1,000 $MWm^{-2}K^{-1}$ 4H-SiC/diamond[67]
SiC (3C)	2.36	500 (ref. 133)	620 $MWm^{-2}K^{-1}$ 3C-SiC/Si[154]
Boron arsenide	1.5	700–1,300 (refs. 168–170)	–
Copper	–	>300	–
Graphene/carbon nanotubes (CNTs)	–	1,300–2,500 (refs. 174–182)	–

The table lists the thermal management materials of interest, the corresponding bandgap, the measured thermal conductivity and the best interface achieved that is documented in the literature. TBC, thermal boundary conductance; TBR: thermal boundary resistance.

Thermal management material candidates

The role of thermal management materials in electronic devices can be either active or passive in terms of how the heat energy is injected or dissipated. The suitability for insertion of thermal management materials in a device architecture depends not only on their thermal conductivity but also on their abilities to conduct or insulate charge carrier flows, described by their bandgap (Table 1). Typically, in an IC, the heat generated from the FEOL devices is evacuated to the semiconducting substrate and the front-side interconnect and power networks, spread to the surrounding dielectric materials and conducted through the thermal interface materials, before it reaches the heat sink and is cooled by the outer environments. The BSPDN-implemented stacked device introduces additional insulating bonding interfaces between the device and a semiconducting carrier wafer, whereas the power delivery networks are relocated to the backside. To improve the overall thermal dissipation in the BSPDN-implemented stacked device, electrical insulating thermal management materials can be inserted to replace the conventional low thermal conductivity BEOL interlayer dielectrics and bonding films. Semiconducting thermal management materials can be inserted as a replacement heat spreader carrier substrate, or even the device semiconductor substrate to mitigate self-heating effects in scaled devices. Conductive or semi-metal thermal management materials can further enhance the thermal dissipation through thermal vias or thermal conductive fillers in thermal interface composite materials (Fig. 1e).

Electrical insulating thermal management materials (bandgap > 5 eV)

Thermal management materials with bandgap above 5 eV, including diamond, aluminium nitride (AlN) and boron nitride (BN), can be regarded as electrical insulators and used as heat-spreading bonding films and low-*k* high thermal conductivity interlayer dielectrics in the BEOL.

Single-crystal diamond. In contrast to sp^2-hybridized carbon allotropes such as carbon nanotubes (CNTs), graphene and graphite, diamond is an sp^3-hybridized carbon material with an isotropic cubic crystal structure. It has a wide bandgap of 5.47 eV and high electron and

hole mobilities (~4,500 and 3,800 $cm^2 V^{-1} s^{-1}$) but low carrier densities at room temperature[20–22]. Unlike sp^2 allotropes, diamond's thermal conduction is isotropic, relying on lattice vibrations. Its strong carbon bonding and light atomic mass result in high phonon frequencies and acoustic velocities[20,23], enabling theoretical thermal conductivity up to 3,500 $W m^{-1} K^{-1}$ at room temperature, making diamond one of the most thermally conductive materials[24].

The thermal conductivity of natural and synthetic single-crystalline diamonds (SCDs) ranges from 1,700 to 2,400 $W m^{-1} K^{-1}$ (refs. 25,26). Defect-induced phonon scattering, rather than intrinsic phonon–phonon scattering, mainly limits these values. Even the best-quality SCDs (2,200–2,400 $W m^{-1} K^{-1}$) contain impurities such as carbon-13, nitrogen and hydrogen, which are difficult to eliminate during growth[27,28]. Linear defects significantly impact thin SCD films, where high dislocation densities (~10^9 cm^{-2})[29–32] cause phonon–dislocation interactions, reducing the thermal conductivity[33,34] and introducing intrinsic stress that complicates integration. Thicker films, typically several hundred micrometres, have lower dislocation densities (10^4–10^6 cm^{-2}) and are preferred for thermal management due to higher conductivity and reduced stress.

The high-pressure high-temperature method and chemical vapour deposition (CVD) are the main techniques for producing SCDs. Although the high-pressure high-temperature method yields high-quality diamonds, it is unlikely to be scaled up for microelectronic application. CVD, especially microwave plasma CVD, is preferred for its scalability and ability to produce large-area diamonds, including films with diameters of several tens of centimetres[35–37].

Currently, SCDs can be grown on two substrates: SCD itself (homoepitaxy) and single-crystal iridium (heteroepitaxy). For homoepitaxy, mosaic growth involves ion implantation, CVD overgrowth, laser cutting, lift-off and assembly of SCD tiles into a monolithic substrate[38–40]. Although mosaic films achieve thermal conductivity exceeding 2,000 $W m^{-1} K^{-1}$, the process is labour-intensive, with alignment and lift-off challenges hindering large-scale production[41–43].

Heteroepitaxy on iridium substrates uses bias-enhanced nucleation[35,44,45], where deposited hydrogenated amorphous carbon forms diamond-like clusters that merge into films with mosaic spreads below 1° (refs. 45–47). Despite this, warping, cracking and the need for high-density plasma restrict film sizes to 100 mm[35,48–51]. To enable larger SCD films, advanced engineering of substrates and CVD chambers is essential.

SCDs face growth challenges and incompatibility with standard IC processes, limiting their use in thermal management. One notable application is integrating SCD films with GaN high electron mobility transistors[52,53], which operate at high frequencies (>100 GHz) and power densities (10 $W mm^{-1}$ at 10 GHz) but are prone to self-heating. SCDs effectively lower device temperatures by serving as heat spreaders, either through bonding or by growing GaN directly on SCD substrates[54]. However, large lattice and thermal expansion mismatches often cause wafer cracking, and the GaN/diamond interface has a high TBR of 20–50 $m^2 K GW^{-1}$ (ref. 55). SCDs are also used as heat sinks for high-power devices[56]. Embedded microchannels in SCD heat sinks enhance heat removal, reducing chip temperatures by up to 42% compared with traditional silicon, copper or aluminium heat sinks[57]. Despite their thermal advantages, the stiffness and chemical inertness of SCDs complicate manufacturing, requiring advancements in processing, integration and scaling for commercial viability.

Polycrystalline diamond. At the atomic scale, polycrystalline diamond (PCD) films have the same fundamental properties as SCD films that give rise to the impressive thermal conductivity of diamond. However, in the polycrystalline case, thermal conductivity is limited primarily by the grain size and boundaries. Grain boundaries limit phonon wavelengths, reducing thermal conductivity in materials. Most PCD films historically exhibited columnar grain structures, where tall, thin grains provide high cross-plane thermal conductivity ($k_\perp$ up to 2,200 $W m^{-1} K^{-1}$ for thick samples) but much lower in-plane thermal conductivity ($k_\parallel$ typically 2–25 times lower)[58–60]. In 2023, isotropically grown PCD achieved similar $k_\perp$ and $k_\parallel$ values, up to 1,600 $W m^{-1} K^{-1}$ depending on the thickness[61]. Beyond blocking phonons, grain boundaries reduce thermal conductivity through two mechanisms: a crystalline mismatch between joined grains, contributing 0.143 $m^2 K GW^{-1}$ of thermal resistance[62]; and the accumulation of sp^2 impurities and other defects, which degrade phase purity and grain boundary quality.

Growth of PCD is most often accomplished with hot filament or microwave plasma-assisted CVD. To prepare substrates for polycrystalline growth, a seeding pretreatment is usually needed to enable nucleation of diamond domains. Depending on the substrate (silicon or GaN), a low percentage of CH_4/H_2 is used as the carbon source and H_2 is used as the activator. Usually, a high-temperature (600–900 °C) environment or high-density plasma is required to convert CH_4 to CH_3^+ and H_2 to H^+ to start the reaction at the surface of the sample. In 2024, high-quality diamond was also be grown at temperatures lower than 400 °C using low-concentration O_2 as the catalyst[63].

At the research level, PCD has been successfully integrated into various high-power and high-frequency devices both directly on devices or bonded to the backside of substrates[64,65]. Maximum channel temperatures can be lowered to 98 °C and mean channel temperatures to 70 °C without compromising device performance[66]. These films can also be grown using interface engineering by introducing interlayers with a measured TBR lower than 1 $m^2 K GW^{-1}$ (ref. 67), markedly lower than typical bonded substrates which are about 10–20 $m^2 K GW^{-1}$ (refs. 68,69).

PCD shows promise but faces two key challenges in device applications. First, large-area PCD growth is still under-explored, with stress and warpage at interfaces posing issues, particularly for larger substrates. Although PCD growth is simpler than SCD due to no lattice matching requirements, these interface problems need resolution. Second, diamond growth requires high temperatures, with current levels as low as 400 °C still too high for temperature-sensitive materials. Further reductions are needed for broader compatibility. Moreover, although interface engineering has advanced, each new material interface requires customized optimization to maximize heat transfer efficiency.

Overall, PCD films are among the most advanced and promising materials being explored for thermal management applications. Although further research and development are required to advance growth techniques and integration methods, PCD already demonstrates essential advantages such as high thermal conductivity and very low TBR with common semiconductor materials, establishing itself as a strong candidate for next-generation electronic devices.

Diamond-like carbon. Among amorphous carbon materials, diamond-like carbon (DLC) exhibits a higher fraction of sp^3-hybridized carbon atoms[70]. If the sp^3 fraction is higher than 70%, the materials are called tetrahedral amorphous carbon (ta-C) or hydrogenated tetrahedral amorphous carbon (ta-C:H)[71]. Because of their high hardness up to tens of gigapascals, DLC films are widely used as coatings to enhance or modulate the mechanical properties of tools and engineering parts[72].

However, because of disorder-induced scattering, DLC films present low thermal conductivity. Depending on the sp^3 fraction, film density and thickness, the value might vary from <1 to ~5 W m^{-1} K^{-1} at room temperature[73,74]. Compared with SCD and PCD counterparts, DLC films might not serve as effective heat spreaders, and thus are not commonly used for thermal management. Still, ongoing research is using DLC to replace existing very low thermal conductivity dielectric films such as mesoporous low-k materials in some microfabrication applications[75]. Nevertheless, for this application, other aspects of the dielectric properties need to be considered in parallel.

Aluminium nitride. AlN stands out as a promising choice for advanced thermal management applications thanks to its high crystalline bulk thermal conductivity (~300 W m^{-1} K^{-1} near room temperature[76–78]), and excellent electrical insulation properties with a wide bandgap of about 6.1 eV[79,80]. Furthermore, AlN exhibits promising BEOL process compatibility[6,10]. Polycrystalline AlN can be deposited on arbitrary substrates at relatively low temperatures (<400 °C) and subsequently planarized and patterned using conventional semiconductor processing schemes. However, the thermal conductivity of AlN can be negatively affected by structural and compositional non-idealities imposed by deposition condition and substrate lattice mismatch.

The reported thermal conductivity of AlN exhibits a broad range, from a few watts per metre per kelvin to approximately 300 W m^{-1} K^{-1}, depending on factors such as deposition conditions, film thickness and the choice of substrate[76,78,81–94] Deposition parameters influence the material's crystallinity, including the grain size and orientation, as well as the presence of vacancies, impurities (such as carbon and oxygen) and defect density[93–95]. These non-idealities contribute to excessive phonon scattering, reducing thermal conductivity from the ideal defect-free single-crystal bulk values. High thermal conductivities (>100 W m^{-1} K^{-1}) in polycrystalline AlN films are often achieved in thick layers (more than a few micrometres) deposited on crystalline, lattice-matched substrates at elevated temperatures (>400 °C)[81,88–90]. A $k_\perp$ value of ~100 W m^{-1} K^{-1} can also be achieved in submicrometre AlN films deposited at low temperatures on both crystalline and amorphous substrates[81–85].

Low-temperature deposition of AlN has been largely studied through sputtering and plasma-enhanced atomic layer deposition[81,84–92,96,97]. Sputter deposition can produce high-quality polycrystalline AlN with thermal conductivities exceeding 100 W m^{-1} K^{-1} for micrometre and submicrometre-thick films[10,85–87,91]. The properties of sputter-deposited AlN films are highly dependent on deposition parameters such as the substrate temperature, sputtering power, deposition pressure and gas composition. These parameters can be finely tuned to achieve uniform coatings with decent control over film thickness, crystallinity and composition[81,85,98–103]. Furthermore, the radio frequency bias used in the sputtering process can drastically affect the surface morphology and grain-to-grain junction quality of the AlN films. A low radio frequency bias condition would result in the formation of triple-junction voids in the film. Suspended AlN cantilever structures with a micro-size gold transducer can be used to evaluate $k_\parallel$ without ambiguity from substrate-dominated heat conduction using micro time-domain thermal reflectance measurements. The $k_\perp$ and $k_\parallel$ values of a 200 °C sputtered AlN film can be as high as 100 W m^{-1} K^{-1} and 40 W m^{-1} K^{-1}, respectively[6]. Despite the high-quality and uniform AlN film deposited by magnetron DC sputtering, the slow deposition rate of a few nanometres per minute can be a potential integration challenge. This manufacturability challenge can be alleviated using high-power impulse magnetron sputtering plus kick, which can significantly increase the deposition rate to about 25 nm min^{-1} (ref. 101).

For submicrometre AlN films, thermal conductance is often limited by poor thermal boundary conductance (TBC) between AlN and the substrate, as well as the lower thermal conductivity of the near-interface transitional AlN layer[90,102]. TBC values between AlN and various substrates, including Si(111), c-Al_2O_3, SiN and SiO_2, typically do not exceed 150 MW m^{-2} K^{-1} (refs. 81,83–87). However, AlN films exhibiting high crystallinity and c-axis texturing near the interface can also achieve notably higher TBC values, approaching 300 MW m^{-2} K^{-1} (refs. 81,85). This improvement in TBC highlights the importance of optimizing the crystalline quality and texture of AlN films for enhanced thermal management.

Despite the demonstrated high thermal conductivities and enhanced TBC discussed earlier, further research is essential to fully determine the mechanisms driving these improvements. Additionally, addressing challenges such as anisotropic thermal conductivity is essential for unlocking the full potential of AlN in advanced IC technology.

Boron nitride. BN is an insulator (bandgap ~6 eV) with high thermal conductivity. BN can exist in many phases, including hexagonal boron nitride (h-BN), cubic boron nitride (c-BN), turbostratic boron nitride (t-BN), rhombic boron nitride (r-BN) and amorphous boron nitride (a-BN). For thermal dissipation, h-BN and c-BN are particularly relevant. Although c-BN has been reported to have higher thermal conductivity, it is less stable than h-BN and is usually grown at higher temperatures and pressures, making it less compatible with 3D IC integration[104,105]. h-BN is a layered 2D material with a honeycomb structure and sp^2 bonding, similar to graphene[106,107]. The boron and nitrogen atoms are covalently bonded in plane, whereas the layered sheets are held together by weak van der Waals forces in the cross-plane direction, leading to anisotropic thermal properties[108,109]. The high thermal conductivity of BN combined with its good mechanical strength, chemical stability, electrical insulation and low dielectric constant make it very promising for thermal management applications in 3D ICs[110,111].

Reports of measured thermal conductivity in h-BN vary widely, depending on the thickness and crystal quality. The measurements for both $k_\perp$ and $k_\parallel$ are often performed with opto-thermal Raman techniques, thermo-reflectance methods or electrothermal methods using suspended microstructures[104,108,109,112–120]. $k_\parallel$ ranges from 220 to 420 W m^{-1} K^{-1} for bulk films and from 200 to 750 W m^{-1} K^{-1} for thinner films, whereas $k_\perp$ is generally <5 W m^{-1} K^{-1} (refs. 107–110,114–117). Thin films of single-crystal h-BN were reported to have higher $k_\parallel$ due to larger grain size and less scattering from reduced interlayer interactions[107,119]. Increased $k_\parallel$ can be obtained modifying the boron isotope concentration, which is attributed to suppression of phonon scattering processes[118–120].

h-BN has been integrated into material stacks and devices to enhance heat dissipation and reduce overall device temperatures[110,111,113]. The widespread adoption of h-BN as a heat spreader in 3D ICs faces several challenges. A key issue is the difficulty in growing large-area h-BN films at BEOL-compatible temperatures while maintaining high crystallinity. To date, most studies use h-BN crystals grown at high temperatures and exfoliated (via mechanical or liquid exfoliation) into micro-scale films, which are then transferred to the target device. Although thin h-BN films grown via CVD offer larger areas and easier integration, these films are often polycrystalline, containing numerous grain boundaries that degrade thermal conductivity.

Another limitation of h-BN lies in its anisotropic thermal conductivity with high $k_{\parallel}$ and low $k_{\perp}$, which reduces the efficiency of vertical heat spreading to the substrate or heat sink in 3D ICs. Efforts to synthesize h-BN nanocomposites featuring isotropic thermal conductivity are ongoing but often result in materials with low overall thermal conductivity[113]. Vertically aligned h-BN films can be fabricated using high-power impulse magnetron sputtering. It was reported that vertically aligned h-BN embedded within a memristor showed improved thermal dissipation, with a threefold increase in the $k_{\perp}$ value[121]. However, the $k_{\perp}$ value of this sputtered material remains relatively low – comparable with conventional SiO_2 – because of suboptimal grain alignment.

Achieving breakthroughs in growing vertically aligned h-BN via scalable techniques such as CVD or physical vapour deposition under BEOL-compatible conditions could unlock new opportunities for h-BN in heat spreader applications. Conversely, the thermal anisotropy of h-BN could be exploited for thermally isolating components in a 3D IC. For instance, h-BN could help isolate stacked memory and logic dies to prevent thermal interference[122,123]. Continued research into optimizing h-BN synthesis methods and tailoring its anisotropic properties will advance its adoption in both heat management and thermal isolation applications.

Semiconducting thermal management materials (1 eV < bandgap < 4 eV)

Semiconducting thermal management materials, such as silicon carbide (SiC) and boron arsenide, with bandgaps ranging from 1 eV to 4 eV, offer versatile applications. They can be used as heat spreaders in far back-end layers where electrical leakage is less critical, as replacement thermal substrates in advanced packaging technologies or even as alternative channel materials to mitigate self-heating effects in scaled devices.

Silicon carbide. SiC is a compound semiconductor with several polymorphs, distinguished by SiC layer stacking along the *c*-axis[124]. The most common polytypes – 3C-SiC, 4H-SiC and 6H-SiC – have bandgap energies of 2.36 eV, 3.26 eV and 3.02 eV, respectively. 3C-SiC, with its cubic structure, is favoured in the semiconductor industry for its compatibility with silicon and higher thermal conductivity. At room temperature, the $k_{\perp}$ values for 4H-SiC and 6H-SiC are approximately 415 W m^{-1} K^{-1} and 345 W m^{-1} K^{-1}, whereas $k_{\parallel}$ values are around 390 and 320 W m^{-1} K^{-1} (refs. 125,126). Isotropic thermal conductivity of 3C-SiC exceeds 500 W m^{-1} K^{-1}, matching theoretical predictions[127]. For thin films several micrometres thick, 3C-SiC achieves $k_{\perp}$ between 200 and 400 W m^{-1} K^{-1}, comparable with or outperforming some PCD films[128].

The modified Lely process, a physical vapour transport method, is used for growing single-crystal 3C-SiC, 4H-SiC and 6H-SiC boules or ingots[129–133]. Although achieving high purity and quality is challenging, 4H-SiC and 6H-SiC wafers up to 150 mm are commercially available, with 200 mm wafers also entering the market. However, producing high-quality bulk 3C-SiC remains difficult due to stacking faults, grain boundaries, anti-phase boundaries and stress[134]. Alternatively, methods such as CVD, magnetron sputtering, alternating supply epitaxy and atomic layer epitaxy have been used to grow SiC thin films[135–141]. Of these, CVD stands out for producing all three polytypes with high quality on silicon or lower-grade SiC substrates, offering promise for large-scale, cost-effective manufacturing[132].

SiC growth temperatures range from 800 to 2,500 °C, making it unsuitable for direct device integration. Instead, SiC is often used as a substrate or bonded to devices for thermal management. For GaN-based transistors, SiC outperforms sapphire and silicon substrates due to its higher thermal conductivity and better lattice matching[142–146]. SiC also supports Ga_2O_3 ultrawide bandgap devices on 4H-SiC substrates, offering excellent thermal performance[147,148]. Additionally, SiC thin films and wafers can serve as interlayers to interface GaN with substrates such as silicon and diamond, improving TBC values substantially compared with direct GaN/Si or GaN/diamond interfaces. High TBC values of around 230–290 MW m^{-2} K^{-1}, >100 MW m^{-2} K^{-1}, 620 MW m^{-2} K^{-1} and >1,000 MW m^{-2} K^{-1} are reported respectively for 4H-SiC/GaN, 4H-SiC/Si, 3C-SiC/Si and 4H-SiC/diamond interfaces, in contrast to GaN/Si and GaN/diamond interfaces that usually present TBC below 100 MW m^{-2} K^{-1} (refs. 69,149–156). SiC interlayers also reduce stress and crack during GaN deposition on silicon[157,158]. Bulk SiC finds use in microchannel heat sinks, surpassing silicon-based options, although patterning challenges due to strong Si–C bonding require advanced plasma etching techniques for reliable results[159–162]. Incorporating SiC nanomaterials into polymers enhances thermal conductivity and combining them with reduced graphene oxide yields even greater heat dissipation improvements[163–167].

Overall, SiC shows substantial promise as a heat spreader or thermal management substrate, particularly when accounting for key factors such as its high thermal conductivity, good lattice matching with many semiconductors and favourable thermal expansion properties. However, to fully harness its potential, significant advancements are needed in the production of high-quality, large-area SiC wafers and thin films. Additionally, further improvements in patterning and fabrication techniques are crucial to enable the widespread adoption and integration of SiC in diverse applications.

Boron arsenide. Boron arsenide is a semiconductor with a cubic zinc-blende structure and a bandgap of ~1.5 eV[168]. Few experimental studies have focused on the thermal properties of single-crystal boron arsenide, reporting thermal conductivities measured around 700–1,300 W m^{-1} K^{-1} (refs. 168–170), the highest reported values of any bulk semiconductor and only lower than diamond (an insulator). The ultrahigh thermal conductivity values are attributed to the large phononic bandgap, resulting in low acoustic-phonon scattering, in addition to long mean free paths[168]. Unlike many high thermal conductive materials, which are often limited by three-phonon scattering, thermal conductivity of boron arsenide is dominated by both three-phonon and four-phonon scattering[168,169].

Thanks to its high isotropic thermal conductivity, which enables heat spreading in all directions, boron arsenide has become a candidate for thermal management of devices. For example, boron arsenide has been integrated as a cooling substrate with high electron mobility transistors, which showed reduced hot spot temperatures compared with diamond or SiC heat spreaders at the same power density[171]. This ability was attributed to the combination of low TBR and high thermal conductivity. However, many challenges remain before the prevalent use of boron arsenide in thermal management applications is possible, including high-quality growth of large single crystals using chemical vapour transport or large area and thin film growth using CVD[168,171]. In addition, the toxicity of arsenic requires precautions that might prevent its widespread use in ICs[172].

Conducting or semi-metal thermal management materials

Conductive or semi-metal thermal management materials such as copper, graphene and CNTs can be considered in applications such as thermal vias, planar heat spreaders or thermal conductive fillers in thermal interface composite materials.

Copper. Among all metals, silver and copper possess both high electrical and thermal conductivities (>300 W m^{-1} K^{-1}). For semiconductor processing, copper has been widely adopted in interconnect technology. In modern high-performance ICs, a thermal via — in which a via acts as a heat pipe that transfers heat from the hot side to the cold side through a punched hole — has been used to enhance heat dissipation, especially in BSPDN-implemented devices and 3D IC processes[173]. The copper through-silicon via (TSV) serves as an effective method for vertical heat dissipation. Two types of TSV are available: the electrically isolated thermal TSV and the electrical TSV. Although the density of the electrical TSV marginally reduces the chip's maximum temperature because of its lack of extension through interlayer dielectric or heat-spreading layers, it can effectively disperse heat to the thermal TSV. However, accommodating a thermal TSV might require a dummy area that could pose compatibility issues with high-density ICs.

Graphene and carbon nanotubes. Graphene is a 2D semi-metal with a hexagonal network of sp^2-bonded carbon atoms. CNTs share this structure but differ geometrically, with graphene rolled into cylindrical tubes. Both materials exhibit covalent bonding in two dimensions, whereas the third dimension relies on weak Van der Waals forces, leading to anisotropic thermal conductivity. In plane, graphene and CNTs show exceptionally high thermal conductivity, whereas cross-plane conductivity is much lower due to limited phonon transfer between layers or nanotubes. This anisotropy is critical for designing materials and devices for heat management, as efficient thermal transfer primarily occurs in the in-plane direction.

Although the high thermal conductivities of CNTs and graphene are well documented, the exact thermal conductivity of 2D monolayer graphene and its size dependence remain debated. Theoretical predictions for room-temperature $k_{\parallel}$ range from 1,300 to 6,600 W m^{-1} K^{-1}, depending on the models[174–178], whereas most measurements yield 1,300–2,500 W m^{-1} K^{-1} for CNTs and single-layer graphene[179–183]. Suspended graphene films show values around 3,000 W m^{-1} K^{-1} for micrometre-scale samples, surpassing diamond, although some studies report lower values due to defects, impurities or methodological issues[181,182]. First-principles calculations suggest a thermal conductivity of 1,300 W m^{-1} K^{-1} for system sizes above 10 µm, below diamond's benchmark[179]. More precise characterization is needed before graphene can be fully utilized for thermal management. On the other hand, its extreme thermal anisotropy limits its application in complex nanostructures, as low $k_{\perp}$ hinders heat spreading between layers.

Despite the debates around the thermal properties in graphene and the anisotropic nature, graphene and CNTs have historically been deployed as fillers within polymeric thermal interface materials as a method for boosting their very low thermal conductivity[184,185]. The introduction of graphene paper in 2014 has enabled its use as a stand-alone thermal material. Graphene paper is formed by depositing subsequent layers of graphene sheets onto a substrate. In its native state, a relatively high thermal conductivity of 20–170 W m^{-1} K^{-1} can be achieved[186]. However, with the addition of annealing, the defects and impurities in the material can be effectively removed, allowing for a near-theoretical thermal conductivity of 1,300–1,400 W m^{-1} K^{-1} (ref. 186).

Challenges in material processing and integration

Enhancing heat transport relies on effectively introducing high thermal conductivity materials at the interface. As of 2025, the application of high thermal conductivity materials in semiconductor integration is limited and primarily focuses on materials development. However, incorporating high thermal conductivity materials presents challenges that include planarization, etching, boundary engineering and bonding. Overcoming these challenges is crucial for unlocking the full potential of high-performance ICs.

High thermal conductivity materials such as diamond, SiC and AlN require a crystalline structure for optimal phonon propagation. Although both single-crystalline and polycrystalline structures are possible, the latter are more practical for integration but come with challenges. For instance, diamond — known for its exceptional thermal conductivity — poses difficulties in device integration due to its hardness and chemical stability. Achieving a flat diamond surface, crucial for integration, is a slow and complex process. Various techniques such as chemical–mechanical planarization, laser polishing and plasma-assisted polishing have been explored for diamond planarization[187,188]. The polishing rate of PCD is extremely low (material removal rate <10 mg h^{-1}), but facet insensitive planarization can still be achieved using slurry that contains high-hardness nanoparticles (Fig. 2a). However, pits appeared on the polished diamond surface due to the embedded voids in the film. The embedded voids are closely related to the non-ideal seeding condition used in PCD film growth[6]. These defects and grain boundaries in PCD can limit thermal conductivity and degrade electrical resistance[189].

Various techniques have been explored for optimizing the integration of diamond and SiC, with a focus on enhancing etching efficiency and performance. These techniques include using a Cr/Ni bilayer metal etch mask for high selectivity to diamond, ultraviolet laser-induced etching with dry oxygen for increased etch rates, inductively coupled plasma reactive ion etching for surface smoothing and reactive ion etching processes[190–196]. Electron cyclotron resonance-assisted microwave plasma reactive ion etching has achieved high etch rates with minimal variation, enabling microsystem patterning[192] (Fig. 2b). UV photoelectrochemical processing of SiC offers a scalable approach for fabricating precise nanoscale structures, whereas the electrochemical etching strategy based on p-dopant implantation enables the fabrication of diverse SiC devices[195,196].

In semiconductor applications, heat transport is typically phonon-dominated, with phonon scattering becoming a primary concern with temperature variations. The quality and bonding strength of the interface can influence vibrational properties and often act as a heat transport bottleneck in nanodevices. The main factors controlling TBR for solid–solid interfaces include the dispersion and density of states (DOS) for energy carriers in the two materials and the region near the interface. Advancements in experimental techniques and computational tools have revealed that interfaces formed with amorphous solids can exhibit high thermal conductance up to 70 MW m^{-2} K^{-1}, challenging the conventional expectation that structural disorder typically leads to low TBC[6] (Fig. 2c,d). This property is attributed to enhanced bridging effects, which result in a greater overlap of the DOS across the materials.

The development of effective bonding techniques for high thermal conductivity materials to substrates is a critical area of research. For example, germanium can be directly bonded to diamond using oxygen plasma activation and NH_3/H_2O_2 cleaning, enhancing heat dissipation in high-speed devices[197]. Similarly, room-temperature bonding of GaN to diamond surfaces with an intermediate SiC layer has successfully reduced surface roughness, a key factor for efficient heat dissipation in GaN-based power devices[198]. In addition, direct bonding of indium phosphide (InP) to diamond heat spreaders through surface activation and low-temperature annealing has demonstrated robust

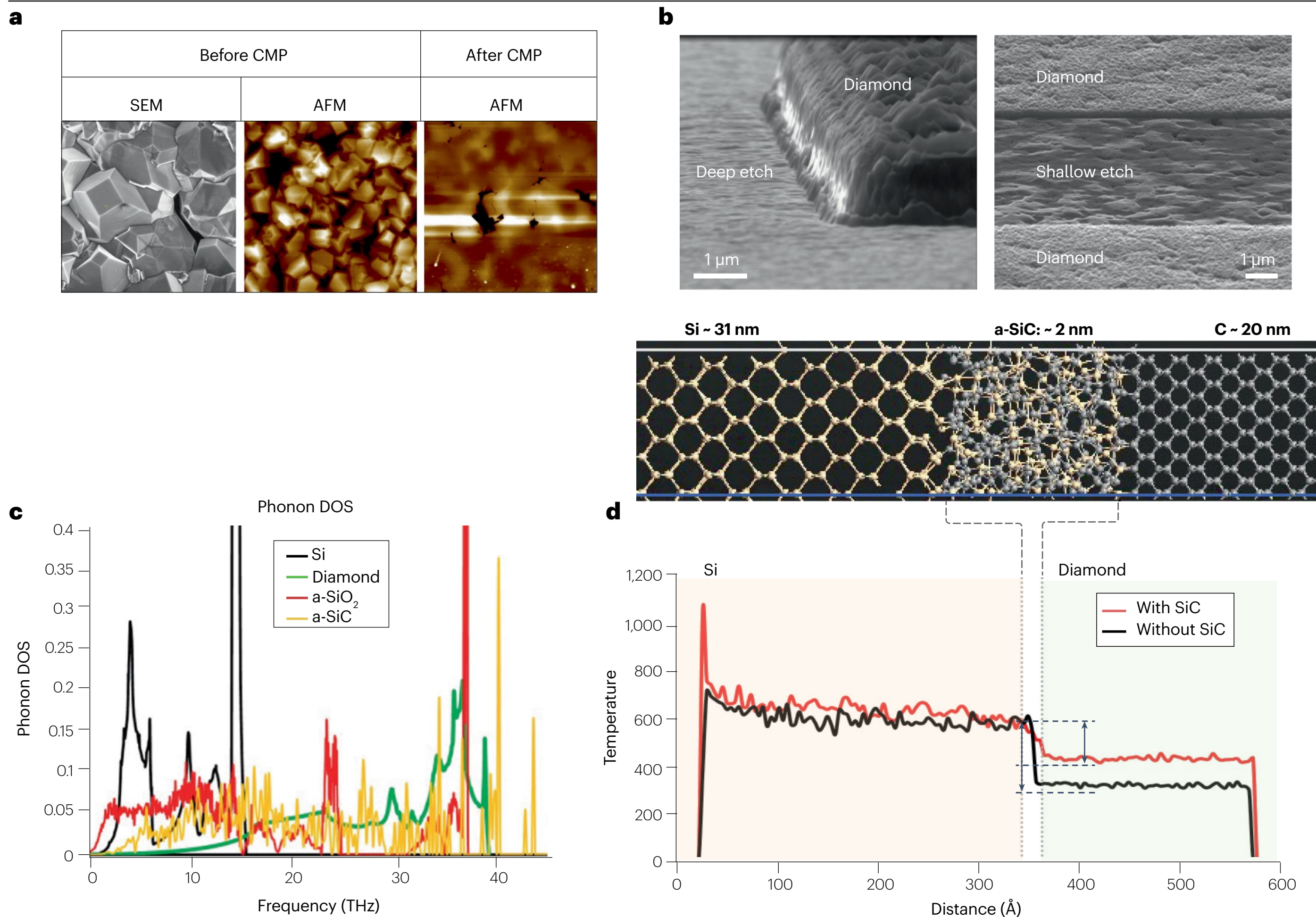


Fig. 2 | Integration challenges of thermal management materials. **a**, Planarization: intrinsic voids in polycrystalline diamond (PCD) are exposed after chemical–mechanical planarization, making it difficult to achieve atomically flat surfaces for bonding. Part **a** is reprinted from ref. 6, IEEE. **b**, Etching: SEM images of etched diamond using high-power (deep etching) and low-power (shallow etching) recipes. Part **b** is reprinted with permission from ref. 6, IEEE. **c**, Thermal boundary resistance (TBR): phonon dispersion relations of diamond (red), silicon (black) and amorphous silicon carbide (SiC) (green), illustrating acoustic mismatch at interfaces. **d**, Simulation: heat transport modelling from silicon to diamond with and without a 2 nm a-SiC bridging layer. The presence of the bridging layer reduces temperature difference across the interface. CMP, chemical–mechanical planarization; DOS, density of states. Part **d** adapted with permission from ref. 10, IEEE.

atomic bonds and improved thermal management for next-generation InP devices[199]. These diverse approaches underscore the adaptability and potential of advanced bonding techniques for a wide range of high-performance applications.

Thermal property measurement

Fundamentally, the main way to measure the thermal properties of a system is to measure its temperature changes under different conditions and to use known physical models to understand the origin of the temperature changes. However, temperature is an emergent statistical phenomenon that describes the average kinetic energy of particles in a system and cannot be measured directly with current measurement tools. As a result, thermal measurement methods are, generally, refined methods for sensing local temperature change through the impacts of increased temperature on either the material under test or the materials adjacent to it. When selecting a thermal measurement method, researchers must consider spatial resolution, sample preparation requirements and measurable thermal properties.

Electrical methods

Almost all electrical methods of thermal property measurement are based on evaluating the thermal coefficient of resistance that describes the relative resistance change that a given material experiences when its temperature changes. Because of the low starting resistance, in metals the change in resistance with temperature is relatively large because of the strong interactions between lattice vibrations and free carrier transport. Furthermore, the resistance change is linear up to 600 °C and down to a thickness of one to three times the electron mean free path when properly prepared[200–202]. It is thus possible to monitor the local temperature using the resistance of metal features such as a patterned pad adjacent to the test material of interest. The electrical methods include thermal interface material testing, heater–sensor/3ω,

transient plane source and scanning thermal microscopy (SThM) techniques. Electrical-based methods usually require non-trivial sample preparation including micrometre scale patterning and fabrication. Moreover, the extraction of thermal conductivity and the corresponding resistance at thermal boundaries using the electrical methods need to carefully consider the complex convolution with the metals used and the precise architecture of the test structures. Nevertheless, electrical methods can be used under dimensions and environments similar to those of commercial microelectronic devices. Therefore, efforts to improve these methods would be meaningful.

Thermal interface material testing. In thermal interface material testing, a material is sandwiched between two metallic cylinders — one cooled and one heated. Metal thermo-resistive thermocouples or other thermal sensors are placed along the length of the cylinder to measure temperature incrementally. The thermal conductivity of the metallic cylinders is known, and the temperature drop across the measurement system is used to calculate the bulk thermal resistance of the material under test. Extracted effective thermal resistance can be coupled with more information about the stack and estimated thermal contact resistances to calculate material thermal conductivity[203,204].

Heater–sensor/3*ω*. In heater–sensor/3ω testing, a thin film metal structure — effectively 1D — is integrated directly onto a sample. This metal structure is designed to have a heating component consisting of a metal film thin enough that joule heating can be used as a source of heat generation, and a sensing component that experiences resistance changes caused by temperature change and can thus be used to sense local temperature. These two components can be separated or integrated into a single structure depending on the specific testing requirements. A more widely adopted 3ω method exploits a phenomenon that occurs when a metal is heated using an alternating current bias with angular frequency ω (Fig. 3). This heating causes joule heating and a resistance change for direct current and 2ω, which then results in a voltage change at a frequency of 3ω. This 3ω voltage change is then amplified, sensed and analysed to extract the thermal conductivity, heat capacity and TBR. The frequency ω is chosen such that the thermal penetration depth — or the depth that the amplitude of the temperature falls to 1/e into the stack — does not interact with the substrate–environment border[205]. The typical frequencies in this measurement method are 0.1 Hz–20 kHz[206]. Typically, a frequency sweep or multi-frequency measurement is conducted to enable maximum data collection and possible parameter extraction. Combined with microfabrication techniques, this method can be embedded in test vehicles of modern semiconductor chips to evaluate the thermal conductivity of films during process development and even serves as a temperature sensor in complex routed circuits[207]. Furthermore, by introducing specially designed test structures such as a suspended cantilever[208], 3ω testing can be a powerful method to measure anisotropy in thermal transport.

Transient plane source. Similar to the 3ω method, transient plane source thermal measurement methods use a structure to act as both a heater and a sensor structure that provides a pulse of heat to the system and senses the thermal resistance change within itself to sense local temperatures which can be used to extract thermal conductivity[209]. Unlike the 3ω method, however, the transient plane source method uses structures that are not directly deposited onto the film but, rather, are mounted on well-characterized adhesives and later attached to the system under test.

Scanning thermal microscopy. SThM is a modification of the contact mode of the atomic force microscopy method that can sense local temperature under a scanning nanometre-scale probe tip. Three main methods of this technique exist: thermo-resistive, 3ω and thermocouple methods. Combined with the temperature map generated using one of the above methods and physical modelling of the stack, it is possible to extract the thermal resistance and TBR of a material[210–212]. Although the measurement time is long, this is the method with the best spatial resolution.

Optical methods

Optical methods for thermal property measurement include thermo-reflectance techniques and other alternatives that probe the temperature change/phonon under irradiation of incident laser beams.

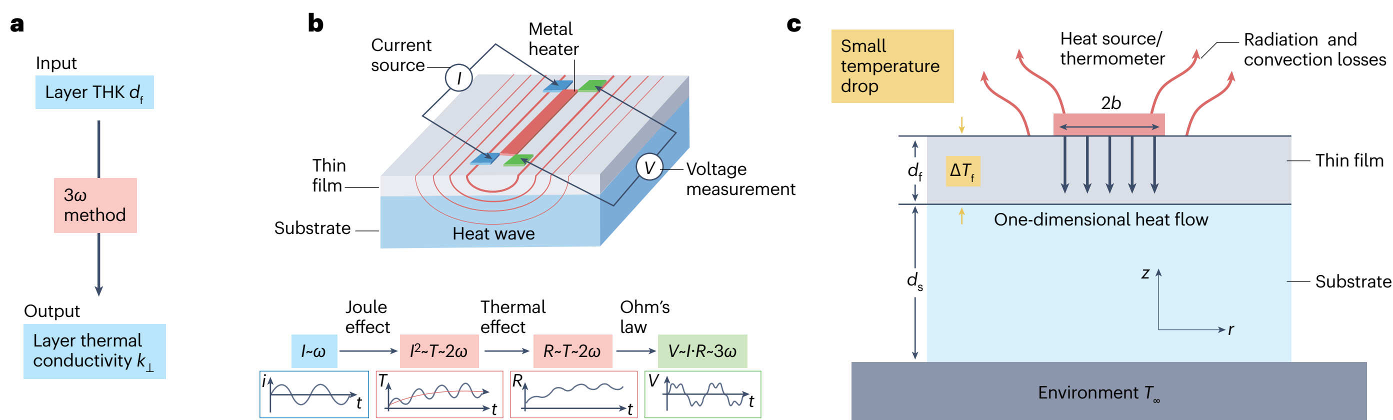


Fig. 3 | Working principle of the 3*ω* method. a, Flow chart of a typical 3ω thermal measurement method. THK, thickness. **b**, Generation of a heat wave from a heated metal pattern caused by an injected electrical current under an electrical bias. This heat then propagates through the thin film and penetrates the substrate (top). The effect of an alternating current (I ~ ω) that generates periodic joule heating (~2ω) that leads to a temperature-induced resistance change and a measurable 3ω voltage signal. This process enables extraction of the thermal conductivity ($\kappa_\perp$) (bottom). **c**, Cross-sectional view of a typical sample used in 3ω measurement. Typical metal heaters are chromium/gold stacks with length 1,000–10,000 µm, width (2b) 20–100 µm and thickness ~400 nm. d_f, thin film thickness; d_s, substrate thickness; ΔT_f, temperature drop across the thin film; T_∞, environment temperature; ω, angular frequency.

Table 2 | Thermo-reflectance methods

Characteristic	TDTR	FDTR	SSTR
Measurement schematic			
Detection principle schematic	Temperature; Time; Pulse heating	Intensity; Periodic heating; Time; Surface temperature; Phase lag	Intensity; Low-frequency heating; Time; Surface temperature; Reflectivity change
Pump/probe source	Picosecond pulsed laser	Continuous wave or pulsed laser	CW laser
Modulation frequency	0.2–20 MHz	0.2–20 MHz	Below kilohertz
Characteristic length scale	Nanometres to micrometres	Nanometres to micrometres	Sub-micrometres to millimetres
Measurement items	$\kappa_{\perp}$, $\kappa_{\parallel}$, TBR	$\kappa_{\perp}$, $\kappa_{\parallel}$, TBR	$\sqrt{\kappa_{\perp}\kappa_{\parallel}}$ (isotropic)

The table reports the measurement schematics, the detection principle schematics, the pump/probe sources, the modulation frequency range, the characteristic length scale and the measurement items that can be acquired for time-domain thermo-reflectance (TDTR), frequency-domain thermo-reflectance (FDTR) and steady-state thermo-reflectance (SSTR). TBR, thermal boundary resistance.

Thermo-reflectance methods. Thermo-reflectance techniques have become highly effective thermometric tools for investigating and measuring the thermal characteristics of various microsystems and bulk materials due to the non-destructive nature and the relatively simpler sample preparation compared with electrical-based methods (Table 2). These techniques use the principle of thermo-reflectance to detect alterations in the reflectivity of common metals, which correspond to changes in temperature within the material being studied.

Time-domain thermo-reflectance (TDTR) incorporates a modulated pump–probe set-up where a pump beam heats up the sample surface at a specific frequency, f. The resulting temperature change on the surface is measured by analysing the alteration in the intensity of a reflected probe beam, as either a function of f or the delay time between the pump and probe pulses, in the case of experiments using short pulses. TDTR involves using short pulses, usually less than a picosecond, to observe the decay of thermo-reflectance over time after heating with a pump pulse[213].

Although also pump–probe based, frequency-domain thermo-reflectance (FDTR) can use either pulsed or continuous wave lasers to monitor the phase shift in thermo-reflectance signals solely as a function of f. When the system goes to further low frequencies, the material being studied reaches a steady-state condition during the modulation event. FDTR measures the phase shift that results from the modulated temperature change at a specific frequency, f[214]. Steady-state thermo-reflectance (SSTR) operates similarly to FDTR, but only in the low-frequency range[215]. It monitors the thermo-reflectance of the surface while increasing the pump power, inducing a Fourier-like response in the material.

In thermal grating spectroscopy, two laser beams are crossed at the sample surface, creating an interference pattern that generates a periodic temperature profile or thermal grating[216]. A third laser beam, the probe, is diffracted by this thermal grating, and the diffracted signal is measured as a function of time. By analysing the decay of the diffracted signal, the in-plane thermal diffusivity of the sample can be determined.

By using laser wavelengths that enable nanoscale optical penetration depths, the thermal penetration depth, $\delta_{thermal}$, can be restricted to the focused spot size or even lower depending on the modulation frequency. In high modulation frequency systems such as TDTR and FDTR, the thermal penetration depth can be written as $\delta_{thermal} = \sqrt{2D/\omega}$, where $D = \kappa/\rho C_p$ is the thermal diffusivity, ρ is the density, and C_p is specific heat capacity. This approximation is commonly used for the penetration depth associated with pump/probe thermo-reflectance experiments and the analysis of thermal conductivity accumulation in various works[217–219]. In SSTR, the penetration depth of pump/probe experiments is limited by the heating radius and can be written as $\delta_{thermal} = r'$, where r' is the effective pump/probe $1/e^2$ radius[220]. However, in real material systems consisting of multiple layers, the descriptor of thermal penetration depth can be greatly impacted by interfacial resistances, heat spreading and the inclusion of a thin metal transducer.

Alternative optical methods

The laser flash analysis (LFA) method (similar to SSTR) is performed by coating both sides of a sample with an absorbing and emitting substance such as graphite, heating the backside of the sample with a laser and tracking the temperature rise and fall on the other side of the sample in response using an infrared detector[221]. The time to half maximum of the temperature rise and sample thickness are used to derive an overall thermal diffusivity for the system.

Raman thermography uses Raman spectroscopy to measure the temperature distribution from phonon scattering in the sample and calculate the thermal conductivity[222]. This method has been widely used for thermal conductivity measurement of 2D materials such as graphene and h-BN.

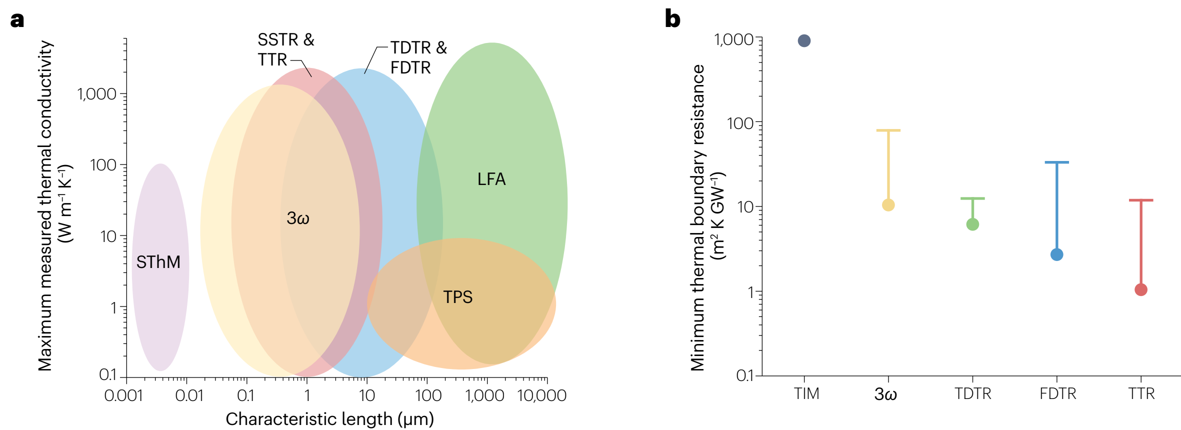


Fig. 4 | Capabilities of thermal characterization techniques. a, Thermal conductivity measurement capabilities as a function of probing thickness ranges (characteristic length) of various thermal characterization methods: scanning thermal microscopy (SThM) (purple), 3ω methods (yellow), steady-state thermo-reflectance (SSTR) and transient thermo-reflectance (TTR) (red), time-domain thermo-reflectance (TDTR) and frequency-domain thermo-reflectance (FDTR) (blue), laser flash analysis (LFA) (green) and transient plane source (TPS) (orange). **b**, The demonstrated minimum measurable thermal boundary resistance (TBR) for typical methods: thermal interface material (TIM) testing (grey), 3ω methods (yellow), TDTR (green), FDTR (blue) and TTR (red). Methods not shown lack reported demonstrations of TBR measurements to the best of our knowledge.

Brief guideline on thermal measurement selection

Electrical methods offer testing under conditions similar to real microelectronic devices, with varying spatial resolutions: thermal interface material testing (millimetre scale), 3ω methods (micrometre scale) and SThM (nanometre scale). Although 3ω methods can measure both in-plane and cross-plane properties, they require complex sample preparation including micropatterning. Optical methods provide non-contact measurements with distinct advantages. TDTR offers excellent temporal resolution (picosecond scale) for thermal conductivity and boundary resistance measurements, and therefore is good for understanding the thermal properties of a submicrometre thin film of interest. FDTR offers tunability in the penetration depth for probing TBRs in a multilayer system. SSTR is particularly suitable for measuring the overall thermal resistance in a complex film stack. For 2D materials, Raman thermography provides unique capabilities but requires transparent samples. The probing thickness ranges and thermal conductivity measurement capabilities of the various thermal characterization methods discussed above are plotted to enable proper selection of thermal characterization techniques to be used for the film stack of interest (Fig. 4a). Furthermore, the comparison of demonstrated minimum measurable TBR for several thermal characterization techniques shows the advantage of thermo-reflectance (Fig. 4b). The ongoing challenge remains developing methods that combine high spatial resolution with accurate interface thermal resistance measurements, particularly for modern bonded interfaces with low TBRs.

Conclusion and outlook

As semiconductor devices continue to scale and adopt complex architectures dominated by 3D integration and nanoscale features, efficient thermal management has emerged as a critical bottleneck. Localized self-heating in densely packed systems demands advanced materials capable of dissipating heat directly at hot spots. Established materials such as diamond, AlN and SiC have demonstrated near-theoretical thermal conductivities, whereas emerging materials such as BN, boron arsenide, graphene and CNTs offer extraordinary heat transport capabilities, making them promising candidates for next-generation solutions.

However, the challenge now lies in moving from material discovery to practical integration into semiconductor manufacturing. Key hurdles include scalable wafer deposition, chemical–mechanical planarization, selective growth, etching processes, bonding techniques and minimizing TBR between layers. Overcoming these barriers is essential to harness the full potential of these materials for modern devices. Complementary advancements in thermal metrology tools are equally critical. Methods such as the 3ω technique and thermo-reflectance approaches are instrumental in characterizing thermal conductivity and TBR at the nanoscale. However, limitations in spatial resolution, throughput, penetration depth and sensitivity must be addressed to enable real-time, high-resolution evaluation in complex device stacks.

The AI era, with its computing clusters expected to consume gigawatts of power, underscores the urgency for scalable and innovative thermal management solutions. Although current cooling strategies such as immersion cooling, direct-to-chip cooling and air cooling are effective, these solutions are insufficient for handling localized heat in compact architectures. The integration of advanced materials into devices offers a transformative opportunity for near-source heat dissipation, improving performance and operational stability.

Looking ahead, a holistic approach combining multiscale modelling, materials development and process innovation will be essential to meet next-generation semiconductor demands. Multiscale modelling can optimize heat transport across atomic-level to system-level scales, whereas improved nanoscale thermal metrology enables accurate characterization and feedback during fabrication. By focusing on integration methodologies and manufacturable solutions, industry can translate breakthroughs in high-performance materials into viable thermal solutions for AI, 3D integration and beyond, ensuring robust performance amid escalating power and thermal requirements.

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Competing interests

The authors declare no competing interests.

Additional information

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